REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

Claims 1-11 and 13-26 are currently pending in the application and subject to examination.

Allowable Subject Matter

As a preliminary matter, the Applicant acknowledges with appreciation the allowance of claims 1-11 and the indication of allowable subject matter in claims 17 and 18.

Claims 13-16 and 19-26 Recite Patentable Subject Matter

In the Office Action mailed September 9, 2004, the Examiner rejected claim 13-16, 19-20 and 24-26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,088,290 to Ohtake et al. and U.S. Patent No. 6,466,075 to Douchi et al. Claims 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohtake et al., Douchi et al. and U.S. Patent No. 6,339,353 to Tomita et al. The Applicant hereby traverses the rejections as follows.

Claims 13, 15 and 16 of the present invention recite a semiconductor integrated circuit comprising, among other features, at least one input buffer that fetches an input signal in synchronization with said internal clock signal provided from said clock buffer.

Claims 19 and 20 of the present invention recite a signal fetching method for fetching input signals "in synchronization with an internal clock signal generated by a clock buffer," comprising, among other steps, activating the clock buffer so that the

"clock buffer generates said internal clock signal, in synchronization with which the input signal[] . . .[is] fetched."

Accordingly, while there is no change in the input signal of the present invention, the internal clock is not generated, thereby saving the power of the clock buffer. The internal clock is generated to fetch the input signal only when the input signal changes. The present invention does not require a separate power down mode signal, like the clock enable signal CKE.

Applicant respectfully submits that the combination of Ohtake et al. and Douchi et al. fails to disclose or suggest at least these features of claims 13, 15, 16, 19 and 20 and that these claims, therefore, recite patentable subject matter.

As the Examiner admits, Ohtake et al. fails to disclose or suggest each and every limitation of claims 13, 15, 16, 19 and 20. In fact, Ohtake et al. fails to teach or suggest at least the limitation of a clock buffer controller that, upon detecting a change in said input signal, activates said clock buffer to generate said internal clock signal and to provide said internal clock signal to said input buffer. *See* Office Action, at page 4.

Applicant respectfully submits that Douchi et al. fails to cure this deficiency in Ohtake et al. Douchi et al. is directed to a clock signal generator that includes two or more clock signal input buffers and an enable signal input buffer. The clock signal generator generates internal clock signals that fluctuate at substantially different timings. However, the relationship between the internal clock signals with respect to validation and invalidation timing remains constant. A latch circuit latches an enable signal from the enable signal buffer in accordance with a first internal clock signal from a first one of the clock signal buffers. A first enable signal connected to the latch circuit

holds the latched enable signal in accordance with the first internal clock signal. A second enable circuit receives the first enable signal and the first internal clock signal and generates a second enable signal used to activate the clock signal buffers. A logic gate receives the first enable signal and the first internal clock signal and controls the output of the first internal clock signal.

Furthermore, in Douchi et al.'s Fig. 4, the clock buffer circuit 10a has a first clock signal buffer 11 and a power-down signal input buffer 13. When the clock enable signal CKE (power-down signal) is at level H, the main power down signal CKEM activates the first clock signal input buffer 11, and when the power down signal CKE is at level L, the main power down signal CKEM deactivates the first clock signal input buffer 11.

The Office Action appears to read the input signal of claim 13 on the power down signal CKE of Douchi et al. According to the Office Action, "[s]ince the technology for implementing a clock buffer controller that activates a clock signal input buffer upon detecting a change in an input signal was well known as evidenced by Douchi, and since a clock buffer controller that activates a clock signal input buffer upon detecting a change in an input signal provides for validation and invalidation timings of the internal clock that changes in accordance with the power-down signal, an artisan would have been motivated to implement the above feature in the system of Ohtake." *See* Office Action, at page 4.

The power down signal input buffer 13 of Douchi et al, however, that fetches the power down signal CKE as the input signal, does not fetch the power down signal CKE in synchronization with the internal clock signal. In claims 13, 15, 16, 19 and 20 of the current invention, the input buffer fetches the input signal based on the internal clock

and the change in this input signal is monitored by the clock buffer controller. According to the present invention, the power down signal CKE is not employed for controlling the clock buffer, but the input signal, that is subject to the internal clock signal, is employed for controlling the clock buffer.

Therefore, the power down signal input buffer 13 of Fig. 4 of of Douchi et al., cannot be read on an input buffer that fetches "an input signal in synchronization with the internal clock signal" as recited in claims 13, 15, 16, 19 and 20.

Alternatively, the Office Action may be attempting to read the latch circuit 14 of Douchi et al. on the input buffer that fetches "an input signal in synchronization with the internal clock signal" of claims 13, 15, 16, 19 and 20 of the current invention. That is, the latch circuit 14 latches the main power down signal CKEMZ based on the first clock signal CLKSZ. Therefore, the Office Action may be attempting to read latch circuit 14 on the input buffer, and the main power down signal CKEMZ, on the input signal. If this is the case, however, Applicant respectfully notes that the trigger clock signal CLKSZ is not controlled by the change of the main power down signal CLKEMZ; it is controlled by the level of main power down signal CLKEMZ. Therefore, when the main power down signal CKEMZ is changed from level H to level L, the first clock signal input buffer 11 is deactivated, not activated. The first input clock signal input buffer 11 is activated by the H level of the main power down signal CKEMZ, and not by the change in the main power down signal CKEMZ.

As disclosed in both Ohtake et al. and Douchi et al., an ordinary DRAM is provided with a power down signal CKE (clock enable) for activating the clock buffer. The current invention, however, does not have the power down signal CKE. Therefore,

the change in the input signal that is fetched by the internal clock is monitored to determine power down mode or not.

For at least these reasons, Applicant submits that claims13, 15, 16, 19 and 20 are allowable over the cited prior art. As claims13, 15, 16, 19 and 20 are allowable, Applicant submits that claims 14, 21, 22, 17, 18 and 23, each of which depends from allowable claims13, 15, 16, 19 and 20, are likewise allowable over the cited prior art.

With regard to claims 24-26, Applicant submits that claims 24-26 are allowable over the cited prior art because the cited prior art discussed above fails to disclose or suggest at least the feature of an input buffer that fetches a command signal or an address signal or the address signal is monitored to detect a change or no change in the signal, as recited in claims 24-26.

For at least these reasons, Applicant submits that claims 24-26 are allowable over the cited prior art.

Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby

authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referring to client-matter number 108066-00038.

Respectfully submitted,

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